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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/613,541	07/07/2000	Atsushi Nakamura	501.34189R00	9061

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/613,541	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/20/03*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/570,646.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Any of claims 26 to 90 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 6, 8, 9, 11 to 30, 34 to 43, 46 to 49, 52 to 56, 59 to 62, 65 to 70, 73 to 76, 79 to 83 and 86 to 90 are rejected under 35 U.S.C. § 102(e) as being anticipated by Akram et al. (U.S. Patent # 5,674,785).

For example, in claim 1 and similar claims 8, 11, 14 and 22, Akram et al. (figures 1 to 11) specifically **figures 1, 1A and 6** show a semiconductor device **10** comprising: a rigid substrate **(12,14 in figure 6)** having a first main surface and a second main surface opposite to the first main surface; a semiconductor pellet **(not label on top of 36b in figure 6,18 in figure 1)** mounted on the first main surface **23** of the rigid substrate, the semiconductor pellet having a plurality of semiconductor circuit elements (inherit) and a plurality of bonding pads **24**; a plurality of electrode pads **14a** formed on the second main surface of the rigid substrate; and a plurality of bonding wires **32** for electrically connecting the bonding pads of the semiconductor pellet with the electrode pads; wherein the semiconductor pellet is mounted facedown on the rigid substrate, the rigid substrate has slits **20** that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, the bonding wires extend through the slits in the rigid substrate to connect the bonding pads and the electrode pads and bump electrodes **16** are formed on said electrode pads.

In claim 2, Akram et al. showing wherein the bonding pads **24** are arranged at the periphery of the semiconductor pellet and the slits **20C** are formed along the directions of rows of the bonding pads **(see figure 1A)**.

In claim 3, Akram et al. show wherein the electrode pads are located on both sides of the slits **20C**.

For example, in claim 26 and similar claims 39, 52, 66, and 80, Akram et al. (figures 1 to 11) specifically **figures 1 and 6** show a semiconductor device comprising: a semiconductor pellet **(not label on top of 36b in figure 6,18 in figure 1)** of a quadrilateral shape having bonding pads **(shown as 24 in figure 1),** formed in a main surface thereof, said semiconductor pellet having a first pair of opposed edges extending in a first direction and a second pair of opposed edges extending in a second direction which intersects said first direction; said bonding pads being arranged in said first direction to form a row of bonding pads; a substrate **(12,14 in figure 6)** having a first surface **(top of 12)**, a second surface **(bottom of 12)** opposite to said first surface, electrode pads formed on

said second surface and a slit **20** passing through said substrate from said first surface to said second surface and extending in said first direction, said semiconductor pellet being disposed on said first surface of said substrate such that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said bonding pads are arranged in said slit in a plan view, said electrode pads including first second electrode pads arranged at the other side of said slit in said second direction; bonding wires **32** electrically connecting said electrode pads of said substrate with said bonding pads of said semiconductor pellet via said slit, said bonding wires including first bonding wires connected to said first electrode pads and second bonding wires connected to said second electrode pads; bump electrodes **16** being disposed on said second surface of said substrate and being electrically connected to said electrode pads of said substrate, said bump electrodes including first bump electrodes electrically connected to said first electrode pads arranged at said one side of said slit and second bump electrodes electrically connected to said second electrode pads and arranged at the other side of said slit, each of said first and second bump electrodes being arranged in both said first and second directions to form a matrix in said plain view, respectively; and a resin sealing body **36B** sealing said bonding wires and said main surface of said semiconductor pellet exposed from said slit.

In claim 27 and similar claims, Akram et al. show said row of bonding pads is disposed at a substantially central area between said first pair of opposed edges of said semiconductor pellets.

In claim 28 and similar claims, Akram et al. show wherein said semiconductor pellet has a rectangular shape, and wherein said first pair of opposed edges correspond to a pair of longer edges and said second pair of opposed edges correspond to a pair of shorter edges.

In claim 29 and similar claims, Akram et al. show wherein said slit tapered so that an opening on said second surface of substrate is greater than an opening on said first surface of said substrate.

In claim 30 and similar claims, Akram et al. show that the bump electrodes are formed of a Pb-Sn alloy.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 1 to 6, 8, 9 and 11 to 25 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hinrichsmeyer et al. (U.S. Patent # 4,996,587).

For example, in claim 1 and similar claims 8, 11, 14 and 22, Hinrichsmeyer et al. (figures 1 to 7) specifically **figure 5** show a semiconductor device **20** comprising: a rigid substrate **10** having a first main surface and a second main surface opposite to the first main surface; a semiconductor pellet **19** mounted on the first main surface **23** of the rigid substrate, the semiconductor pellet having a plurality of semiconductor circuit elements (inherit) and a plurality of bonding pads **21**; a plurality of electrode pads formed on the second main surface of the rigid substrate; and a plurality of bonding wires **22** for electrically connecting the bonding pads of the semiconductor pellet with the electrode pads; wherein the semiconductor pellet is mounted facedown on the rigid substrate, the rigid substrate has slits **13** that extend from the first main surface to the second main surface and expose the bonding pads of the semiconductor pellet, the bonding wires extend through the slits in the rigid substrate to connect the bonding pads and the electrode pads and bump electrodes **25** are formed on said electrode pads.

In claim 2, Hinrichsmeyer et al. showing wherein the bonding pads **21** are arranged at the periphery of the semiconductor pellet and the slits **13** are formed along the directions of rows of the bonding pads.

In claim 3, Hinrichsmeyer et al. show wherein the electrode pads are located on both sides of the slits **13**.

Claims 26 to 29, 33, 34, 35, 36, 42, 46, 48 to 56, 59, 61 to 69, 73, 75 to 82 and 86 to 90 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinrichsmeyer et al. (U.S. Patent # 4,996,587).

For example, in claim 26 and similar claims 39, 52, 66, and 80, Hinrichsmeyer et al. (figures 1 to 7) specifically **figure 5** show a semiconductor device **20** comprising: a semiconductor pellet **19** of a quadrilateral shape having bonding pads **21** formed in a main surface thereof, said semiconductor pellet

having a first pair of opposed edges extending in a first direction and a second pair of opposed edges extending in a second direction which intersects said first direction, wherein at least some of said bonding pads **21** extend in said first direction to form a row bonding pads; a substrate **10** having a first surface, a second surface opposite to said first surface, electrode pads formed on said second surface and a slit **13** passing through said substrate from said first surface to said second surface and extending in said first direction, said semiconductor pellet being disposed on said first surface of said substrate such that said main surface of said semiconductor pellet is faced to said first surface of said substrate and said bonding pads are arranged in said slit in a plan view, said electrode pads including first second electrode pads arranged at the other side of said slit in said second direction; bonding wires **22** electrically connecting said electrode pads of said substrate with said bonding pads of said semiconductor pellet via said slit, said bonding wires including first bonding wires connected to said first electrode pads and second bonding wires connected to said second electrode pads; bump electrodes **25** being disposed on said second surface of said substrate and being electrically connected to said electrode pads of said substrate, said bump electrodes including first bump electrodes electrically connected to said first electrode pads arranged at said one side of said slit and second bump electrodes electrically connected to said second electrode pads and arranged at the other side of said slit; and a resin sealing body **28** sealing said bonding wires and said main surface of said semiconductor pellet exposed from said slit. Hinrichsmeyer et al. fail to explicitly show each of said first and second bump electrodes being arranged in both said first and second directions to form a matrix in said plain view, respectively. However, Hinrichsmeyer et al. (figure 4) does discloses each of said first and second external card connection means **17** being arranged in both said first and second directions to form a matrix in said plain view of the second surface **12** of the substrate **10**, respectively. The external card connection means **17** including first external card connection means electrically connected to said first electrode pads **17a** arranged at said one side of said slit and second external card connection means electrically connected to said second electrode pads **17a** and arranged at the other side of said slit **13**. It is understood to one of ordinary skill in the art, viewing figures 4 and 5, that the solder pad **25** (in which can be considered bumps or balls) on the second surface **12** of the substrate **10** are directly connected to the pattern, row

or matrix of external card connection means **17** shown in the plan view of figure 4. Therefore, it would be obvious to one of ordinary skill in the art to use the teaching of Hinrichsmeyer et al.'s external card connection means and the solder pads to be the claimed bump electrodes to form a matrix as claimed by Applicant for the purpose of providing a electrical connection for the package having a minimum thickness and good thermal qualities whose production can be simplified.

In claim 27, Hinrichsmeyer et al. show said row of bonding pads **21** is disposed at a substantially central area between said first pair of opposed edges of said semiconductor pellets.

In claim 28, Hinrichsmeyer et al. show wherein said semiconductor pellet **19** has a rectangular shape, and wherein said first pair of opposed edges correspond to a pair of longer edges and said second pair of opposed edges correspond to a pair of shorter edges.

In claim 29, Hinrichsmeyer et al. show wherein said slit **13** tapered so that an opening on said second surface of substrate is greater than an opening on said first surface of said substrate.

In claim 34, Hinrichsmeyer et al. show wherein said substrate has land portions **12** and conductors **12** formed between said land portions and said electrode pads **21**, wherein a width of each of said lead portions is larger than a width of each of said conductors, wherein said land portions, said conductors and said electrode pads are integrally formed with one another on said second surface of said substrate, and wherein said bump electrodes are disposed on said land portions, respectively

In claim 35, Hinrichsmeyer et al. show wherein said substrate **10** is formed of a single layer structure that has conductors arranged only on said second surface of said substrate.

Initially, and with respect to claims 33, 46, 59, and 73, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product

produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 7, 10, 31, 32, 33, 37, 38, 44, 45, 50, 51, 57, 58, 63, 64, 71, 72, 77, 78, 84 and 85 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram et al. (U.S. Patent # 5,674,785) in view of Masukawa (U.S. Patent # 5,753,974).

Akram et al. show the features of the claimed invention as detailed above to fail to explicitly show said substrate **4** is formed of a glass fiber impregnated with epoxy resin.

Masukawa is cited for showing an electronic device assembly. Specifically, Massukawa (figures 1A to 7) specifically figures 6A and 6B discloses Masukawa show wherein said substrate **4** is formed of a glass fiber impregnated with epoxy resin (see column 2, lines 65-67) for the purpose of enhancing the lifetime and reliability of a connection between a chip and a substrate.

In claim 33 and similar claims, Masukawa show wherein said bonding wires **5** are formed of gold (see column 4, lines 5-10).

In claim 37 and similar claims, Masukawa show wherein said substrate **4,3** has a periphery which protrudes outwardly from said first and second pairs of opposed edges of said semiconductor pellet **1**, wherein said first surface of said periphery of said substrate and said semiconductor pellet are sealed with a resin sealing body **10**, and wherein a rear surface (back of 1) of said semiconductor pellet opposite to said main surface is exposed from said resin sealing body.

In claim 38 and similar claims, Masukawa show wherein said bumps electrodes **9** are arranged on said second surface of said substrate **(bottom of 4,3)** that overlaps with said semiconductor pellet in said plane view and on said second surface of substrate at said periphery.

Therefore, it would be obvious to one of ordinary skill at the time of the invetion to use Masukawa's glass impregnated substrate and features to modify Akram et al.'s substrate and features for the purpose of enhancing the lifetime and reliability of a connection between a chip and a substrate.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Initially, and with respect to claims 33, 46, 59 and 73, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 33, 46, 59 and 73 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram et al. (U.S. Patent # 5,674,785).

As to the grounds of rejection under section 103, see MPEP § 2113.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 7, 10, 31, 32, 33, 37, 38, 44, 45, 50, 51, 57, 58, 63, 64, 71, 72, 77, 78, 84 and 85 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hinrichsmeyer et al. (U.S. Patent # 4,996,587) in view of Masukawa (U.S. Patent # 5,753,974).

Hinrichsmeyer et al. show the features of the claimed invention as detailed above to fail to explicitly show said substrate **4** is formed of a glass fiber impregnated with epoxy resin.

Masukawa is cited for showing an electronic device assembly. Specifically, Massukawa (figures 1A to 7) specifically figures 6A and 6B discloses Masukawa show wherein said substrate **4** is formed of a glass fiber impregnated with epoxy resin (see column 2, lines 65-67) for the purpose of enhancing the lifetime and reliability of a connection between a chip and a substrate.

In claim 33, Masukawa show wherein said bonding wires **5** are formed of gold (see column 4, lines 5-10).

In claim 37, Masukawa show wherein said substrate **4,3** has a periphery which protrudes outwardly from said first and second pairs of opposed edges of said semiconductor pellet **1**, wherein said first surface of said periphery of said substrate and said semiconductor pellet are sealed with a resin sealing body **10**, and wherein a rear surface (back of 1) of said semiconductor pellet opposite to said main surface is exposed from said resin sealing body.

In claim 38, Masukawa show wherein said bumps electrodes **9** are arranged on said second surface of said substrate **(bottom of 4,3)** that overlaps with said semiconductor pellet in said plane view and on said second surface of substrate at said periphery.

Therefore, it would be obvious to one of ordinary skill at the time of the invetion to use Masukawa's glass impregnated substrate and features to modify Hinrichsmeyer et al.'s substrate and features for the purpose of enhancing the lifetime and reliability of a connection between a chip and a substrate.

Response

Applicant's arguments filed 10/20/03 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

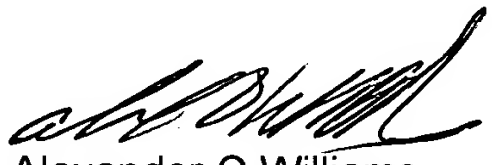
The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,777,780,737,784,673,696,698,680,773	5/14/03 1/19/05
Other Documentation: foreign patents and literature in 257/778,777,780,737,784,673,696,698,680,773	5/14/03 1/19/05
Electronic data base(s): U.S. Patents EAST	5/14/03 1/19/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/20/05